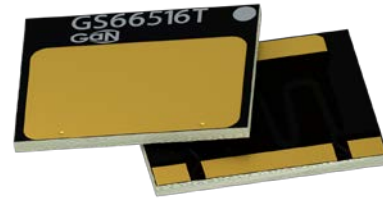
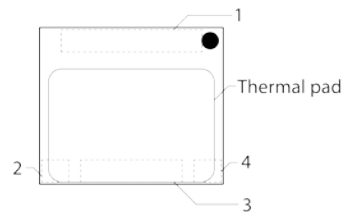


## Features

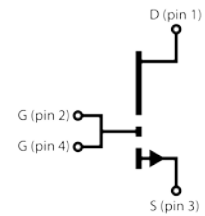
- 650 V enhancement mode power switch
- Top-side cooled configuration
- $R_{DS(on)} = 25 \text{ m}\Omega$
- $I_{DS(max)} = 60 \text{ A}$
- Ultra-low FOM Island Technology™ die
- Low inductance GaN $Px$ ® package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 / +10 V)
- Very high switching frequency (> 100 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 9 x 7.6 mm<sup>2</sup> PCB footprint
- Dual gate pads for optimal board layout
- RoHS 6 compliant



### Package Outline



### Circuit Symbol



*The thermal pad is internally connected to Source (S- pin 3) and substrate*

## Applications

- High efficiency power conversion
- High density power conversion
- AC-DC Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Industrial Motor Drives
- Single and 3Φ inverter legs
- Solar and Wind Power
- Fast Battery Charging
- DC-DC converters
- On Board Battery Chargers
- Traction Drive

## Description

The GS66516T is an enhancement mode GaN-on-silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems implements patented **Island Technology**® cell layout for high-current die performance & yield. **GaN $Px$** ® packaging enables low inductance & low thermal resistance in a small package. The GS66516T is a top-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

### Absolute Maximum Ratings ( $T_{case} = 25\text{ }^{\circ}\text{C}$ except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	$T_J$	-55 to +150	$^{\circ}\text{C}$
Storage Temperature Range	$T_S$	-55 to +150	$^{\circ}\text{C}$
Drain-to-Source Voltage	$V_{DS}$	650	V
Transient Drain-to-Source Voltage (note 1)	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	$V_{GS}$	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current ( $T_{case}=25\text{ }^{\circ}\text{C}$ ) (note 2)	$I_{DS}$	60	A
Continuous Drain Current ( $T_{case}=100\text{ }^{\circ}\text{C}$ ) (note 2)	$I_{DS}$	47	A

(1) Pulse  $\leq 1\text{ }\mu\text{s}$

(2) Limited by saturation

### Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case)	$R_{\theta JC}$	0.3	$^{\circ}\text{C}/\text{W}$
Thermal Resistance (junction-to-board)	$R_{\theta JB}$	3.0	$^{\circ}\text{C}/\text{W}$
Maximum Soldering Temperature (MSL3 rated)	$T_{SOLD}$	260	$^{\circ}\text{C}$

### Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS66516T-TR	GaN $PX^{\circ}$ Top-Side Cooled	Tape-and-Reel	2000	13" (330mm)	16mm
GS66516T-MR	GaN $PX^{\circ}$ Top-Side Cooled	Mini-Reel	250	7" (180mm)	16mm

Electrical Characteristics (Typical values at  $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{GS} = 6\text{ V}$  unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$BV_{DS}$	650			V	$V_{GS} = 0\text{ V}$ $I_{DSS} = 100\text{ }\mu\text{A}$
Drain-to-Source On Resistance	$R_{DS(on)}$		25	32	m $\Omega$	$V_{GS} = 6\text{ V}$ $T_J = 25\text{ }^\circ\text{C}$ $I_{DS} = 18\text{ A}$
Drain-to-Source On Resistance	$R_{DS(on)}$		65		m $\Omega$	$V_{GS} = 6\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ $I_{DS} = 18\text{ A}$
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.3		V	$V_{DS} = V_{GS}$ $I_{DS} = 14\text{ mA}$
Gate-to-Source Current	$I_{GS}$		320		$\mu\text{A}$	$V_{GS} = 6\text{ V}$ , $V_{DS} = 0\text{ V}$
Gate Plateau Voltage	$V_{plat}$		3.0		V	$V_{DS} = 400\text{ V}$ $I_{DS} = 60\text{ A}$
Drain-to-Source Leakage Current	$I_{DSS}$		4	100	$\mu\text{A}$	$V_{DS} = 650\text{ V}$ $V_{GS} = 0\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$
Drain-to-Source Leakage Current	$I_{DSS}$		800		$\mu\text{A}$	$V_{DS} = 650\text{ V}$ $V_{GS} = 0\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$
Internal Gate Resistance	$R_G$		0.34		$\Omega$	$f = 1\text{ MHz}$ , open drain
Input Capacitance	$C_{ISS}$		520		pF	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$
Output Capacitance	$C_{OSS}$		130		pF	
Reverse Transfer Capacitance	$C_{RSS}$		4		pF	
Effective Output Capacitance Energy Related (Note 3)	$C_{O(ER)}$		177		pF	$V_{GS} = 0\text{ V}$ $V_{DS} = 0\text{ to }400\text{ V}$
Effective Output Capacitance Time Related (Note 4)	$C_{O(TR)}$		284		pF	
Total Gate Charge	$Q_G$		12.1		nC	$V_{GS} = 0\text{ to }6\text{ V}$ $V_{DS} = 400\text{ V}$
Gate-to-Source Charge	$Q_{GS}$		4.4		nC	
Gate-to-Drain Charge	$Q_{GD}$		3.4		nC	
Output Charge	$Q_{OSS}$		113		nC	$V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$
Reverse Recovery Charge	$Q_{RR}$		0		nC	

(3)  $C_{O(ER)}$  is the fixed capacitance that would give the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 V to the stated  $V_{DS}$

(4)  $C_{O(TR)}$  is the fixed capacitance that would give the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 V to the stated  $V_{DS}$ .

**Electrical Characteristics continued** (Typical values at  $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{GS} = 6\text{ V}$  unless otherwise noted)

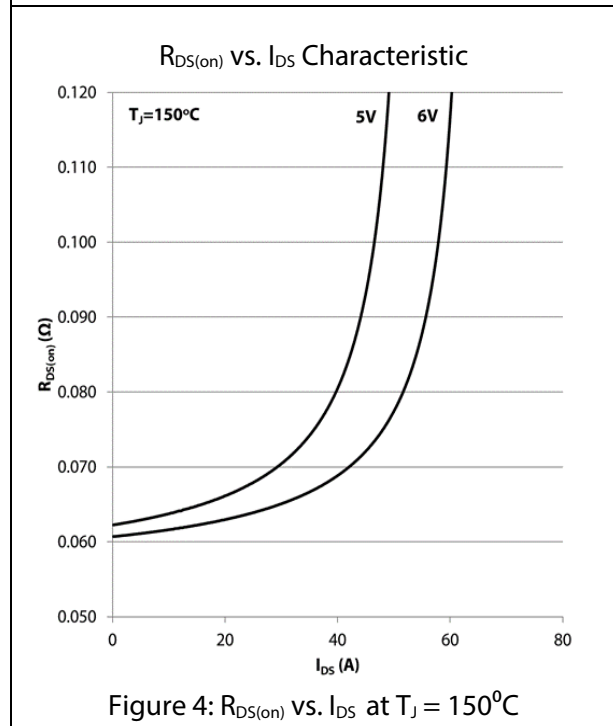
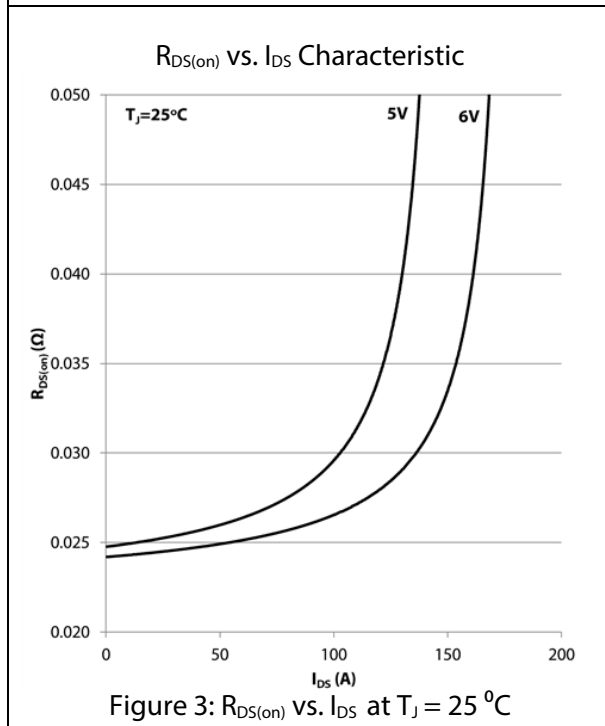
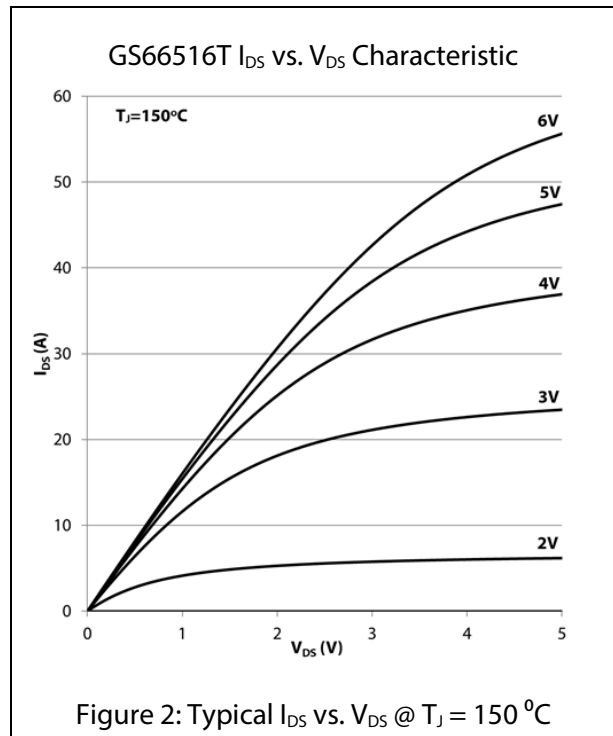
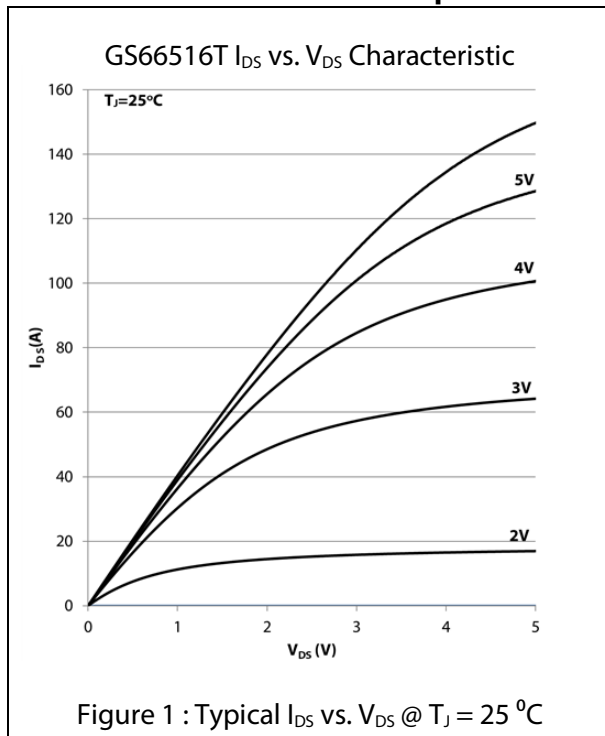
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		4.6		ns	$V_{DD} = 400\text{ V}$ $V_{GS} = 0 - 6\text{ V}$ $I_D = 16\text{ A}$ , $R_{G(ext)} = 5\ \Omega$ $T_J = 25\text{ }^\circ\text{C}$ (note 5)
Rise Time	$t_R$		12.4		ns	
Turn-Off Delay	$t_{D(off)}$		14.9		ns	
Fall Time	$t_F$		22		ns	
Output Capacitance Stored Energy	$E_{OSS}$		14.1		$\mu\text{J}$	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$
Switching Energy during turn-on	$E_{on}$		134.1		$\mu\text{J}$	$V_{DS} = 400\text{ V}$ , $I_{DS} = 20\text{ A}$ $V_{GS} = 0-6\text{ V}$ $R_{G(on)} = 10\ \Omega$ , $R_{G(off)} = 1\ \Omega$ $L = 120\ \mu\text{H}$ $L_P = 10\text{ nH}$ (notes 6, 7)
Switching Energy during turn-off	$E_{off}$		14.7		$\mu\text{J}$	

(5) See Figure 12 for timing test circuit diagram and definition waveforms

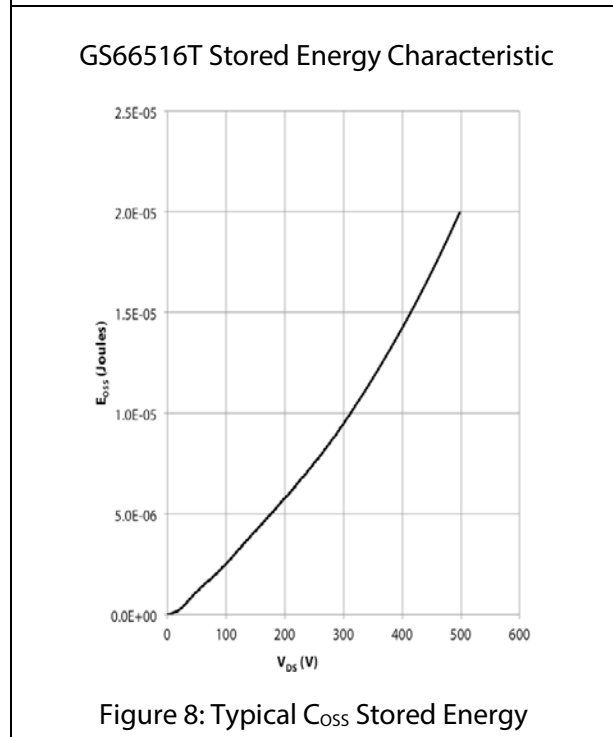
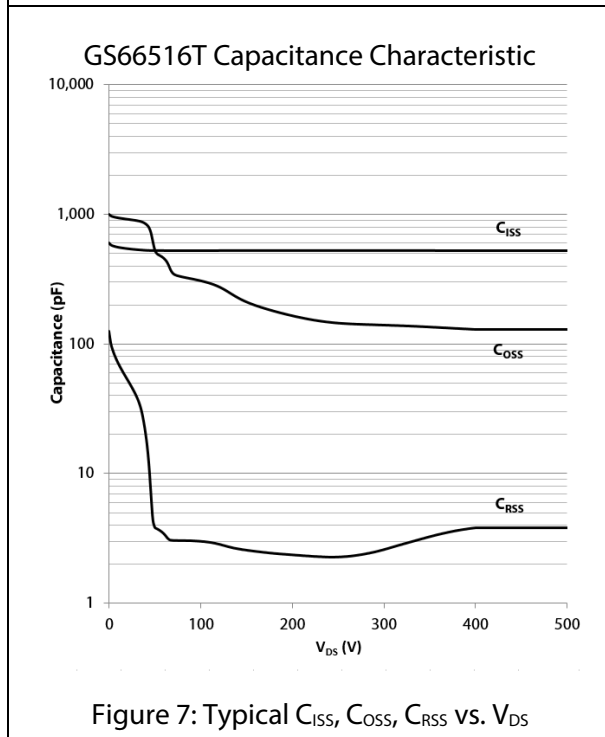
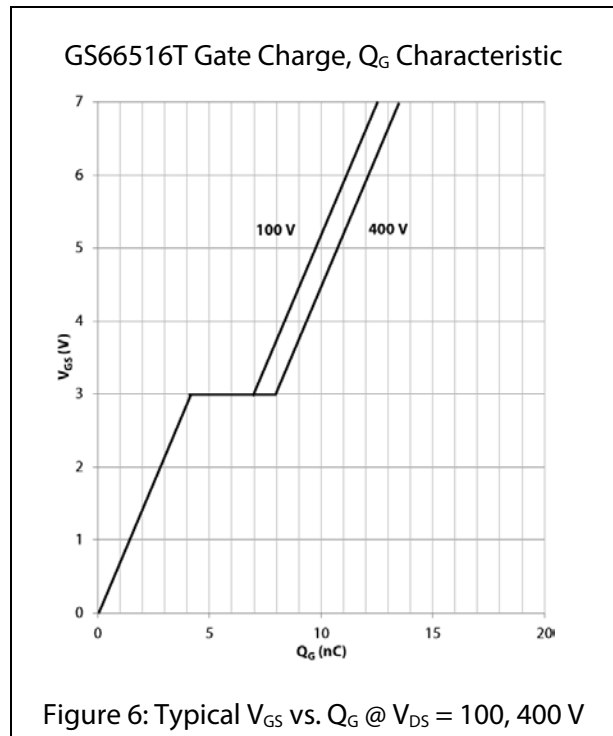
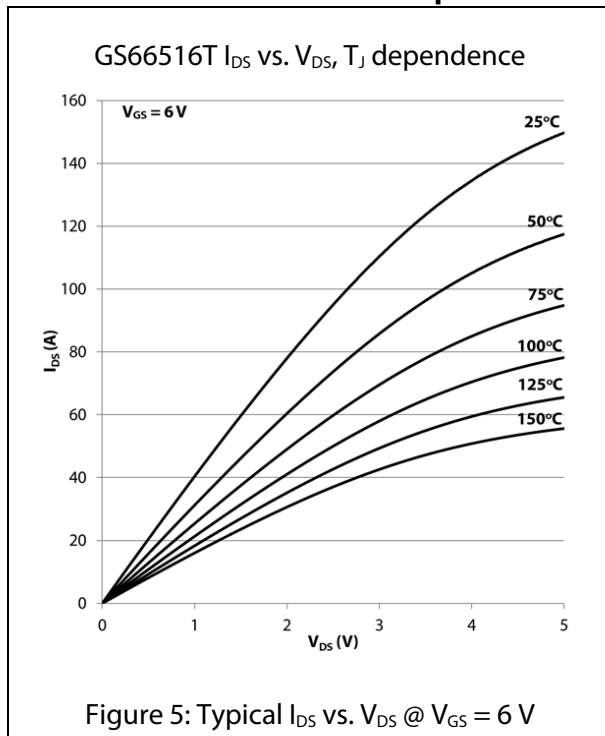
(6)  $L_P$  = parasitic inductance

(7) See Figure 13 for switching test circuit

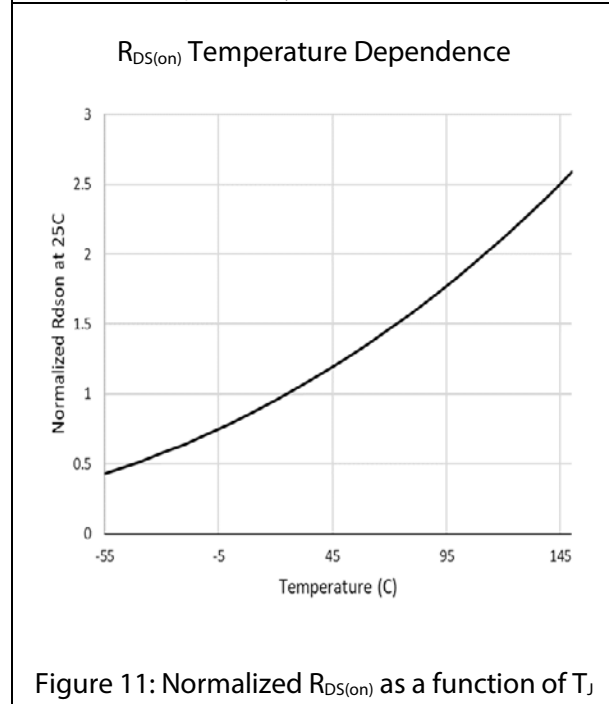
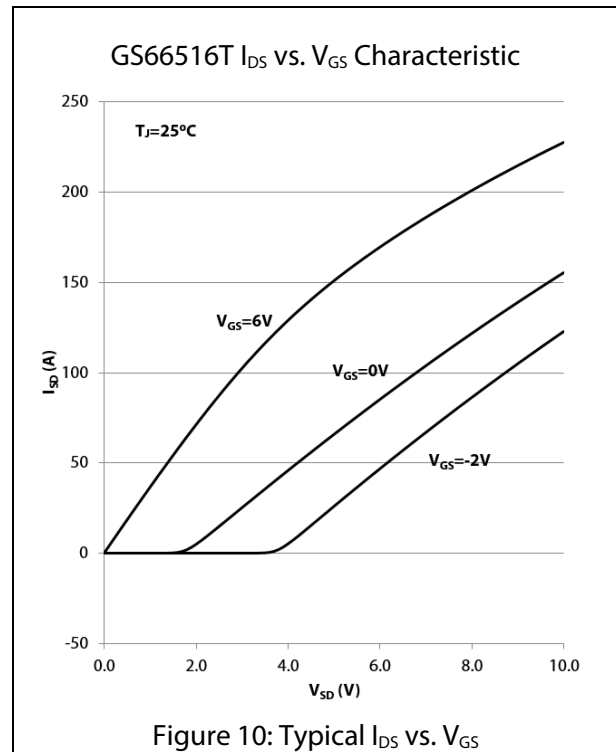
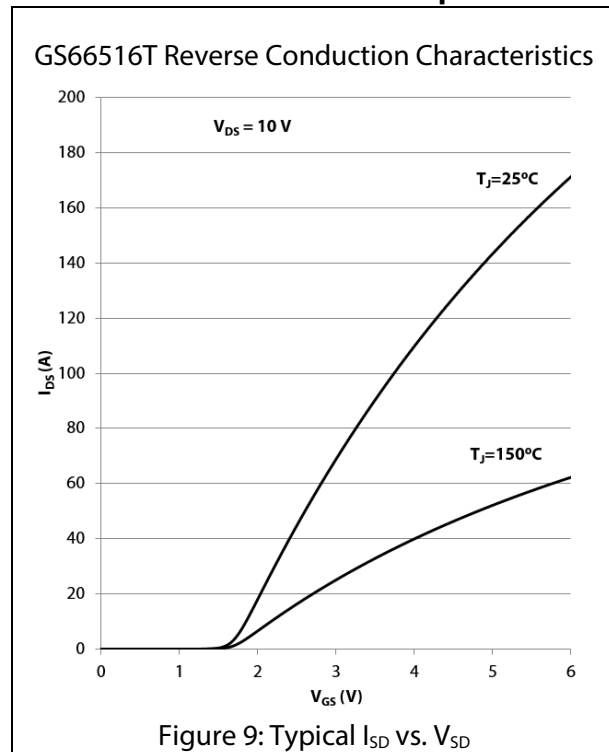
**Electrical Performance Graphs**



**Electrical Performance Graphs**



### Electrical Performance Graphs



**Test Circuits**

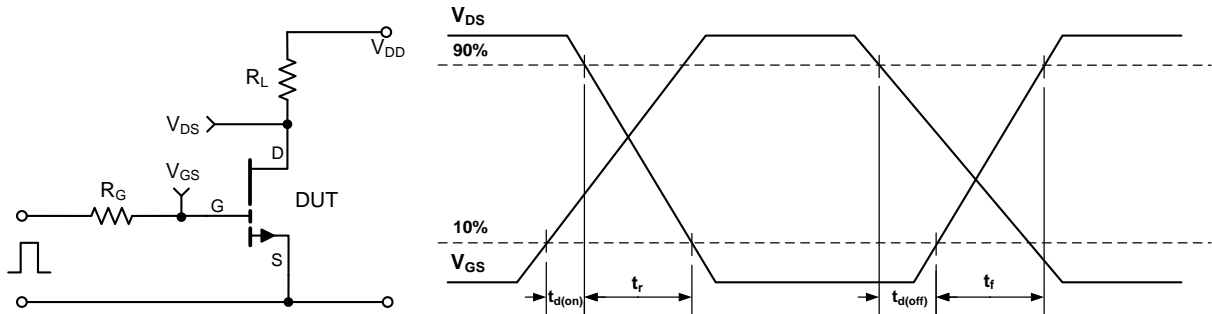
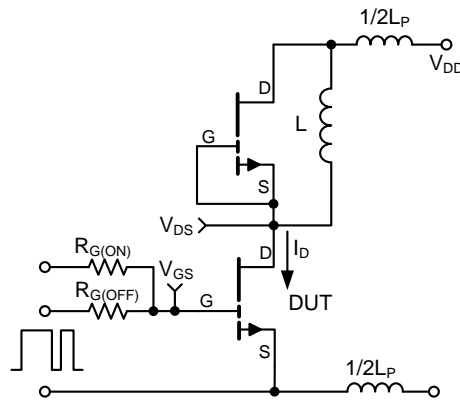


Figure 12: GS66516T switching time test circuit and waveforms





**Thermal Performance Graphs**

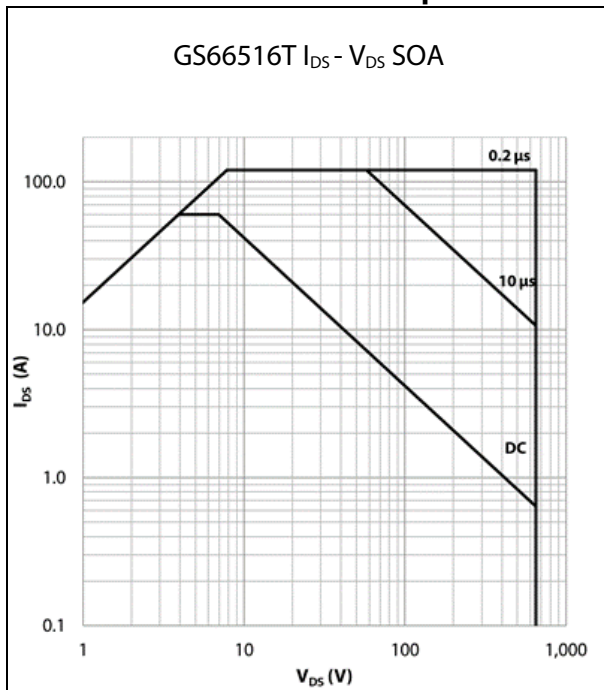


Figure 14: Safe Operating Area @  $T_{case} = 25\text{ }^{\circ}\text{C}$

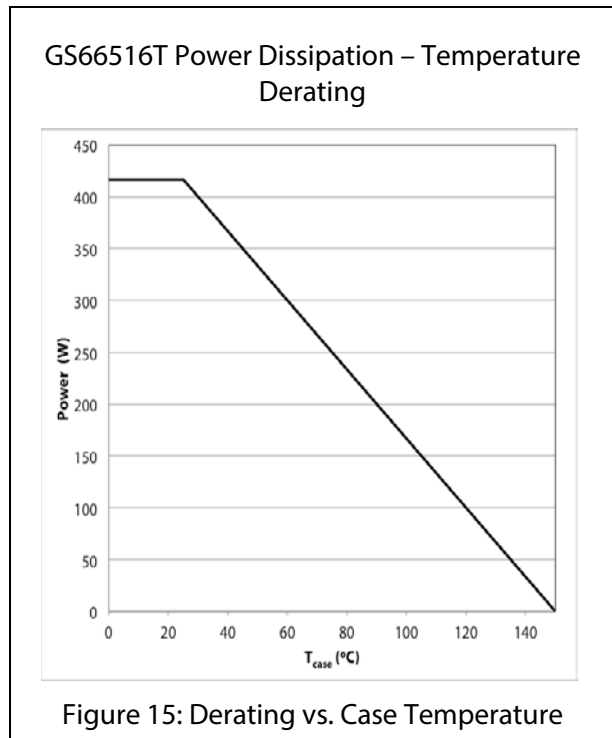


Figure 15: Derating vs. Case Temperature

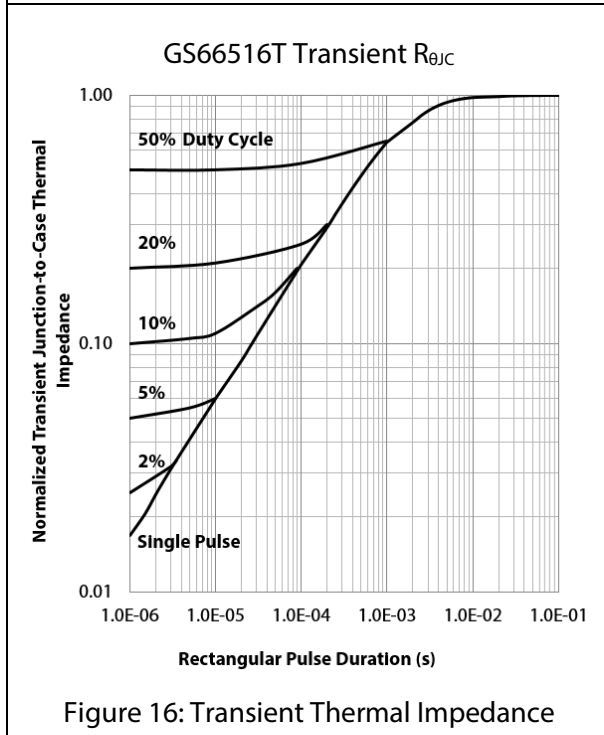


Figure 16: Transient Thermal Impedance

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## Application Information

### Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal  $R_{DS(on)}$  performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1  $\mu$ s. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate, however it increases the reverse conduction loss. For more details, please refer to the gate driver application note "GN001 How to Drive GaN Enhancement Mode Power Switching Transistors" at [www.gansystems.com](http://www.gansystems.com)

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance,  $R_{G(OFF)}$  is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower  $Q_G$  when compared to equally sized  $R_{DS(on)}$  MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Please see the gate driver application note (GN001) for more details.

### Parallel Operation

The dual gate drive pins are used to achieve balanced gate drive, especially useful in parallel GaN transistors operation. Both gate drive pins are internally connected to the gate, so only one needs to be connected. Connecting both may lead to timing improvements at very high frequencies. The two gates on the GS66516T top-side cooled device are not designed to be used as a signal pass-through. When multiple devices are used in parallel, it is not recommended to use one gate connection to the other (on the same transistor) as a signal path for the gate drive to the next device. Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible. GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2  $\Omega$ ) on each gate is strongly recommended to minimize the gate parasitic oscillation.

### Source Sensing

Although the GS66516T does not have a dedicated source sense pin, the GaN<sup>PX</sup>® packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated “source sense” connection on the PCB to the Source pad in a kelvin configuration, the function can easily be implemented. It is recommended to implement a “source sense” connection to improve drive performance.

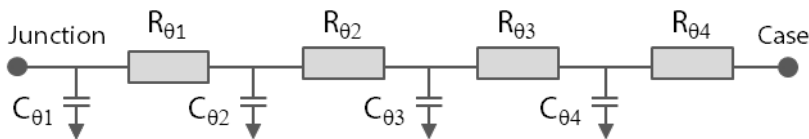
### Thermal

The substrate is internally connected to the thermal pad on the top-side and to the source pin on the bottom side of the GS66516T. The transistor is designed to be cooled using a heat sink on the top of the device. The Drain and Source pads are not as thermally conductive as a thermal pad. However, adding more copper under these two pads will improve thermal performance by reducing the packaging temperature.

### Thermal Modeling

RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra  $R_{\theta}$  and  $C_{\theta}$  to simulate the Thermal Interface Material (TIM) or Heatsink.

The RC elements are assigned to the internal layers of the GS66516T as follows



RC breakdown of  $R_{\theta JC}$

$R_{\theta}$ ( $^{\circ}\text{C}/\text{W}$ )	$C_{\theta}$ ( $\text{W}\cdot\text{s}/^{\circ}\text{C}$ )	Device Layer
$R_{\theta 1} = 0.00\text{T}$	$C_{\theta 1} = 8.03\text{E-}05$	GaN
$R_{\theta 2} = 0.139$	$C_{\theta 2} = 5.59\text{E-}03$	Si
$R_{\theta 3} = 0.140$	$C_{\theta 3} = 1.26\text{E-}03$	Attachment
$R_{\theta 4} = 0.014$	$C_{\theta 4} = 1.90\text{E-}03$	Cu Base

For more detail, please refer to Application Note GN007 “Modeling Thermal Behavior of GaN Systems’ GaN<sup>PX</sup>™ Using RC Thermal SPICE Models” available at [www.gansystems.com](http://www.gansystems.com)

### Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition ( $V_{GS} = +6$  V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance,  $R_{DS(on)}$ , similar to forward conduction operation.

Off-state condition ( $V_{GS} \leq 0$  V): The reverse characteristics in the off-state are different from silicon MOSFET as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, ( $V_{GD}$ ) exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a “body diode” with slightly higher  $V_F$  and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than  $V_{GS(th)} + V_{GS(off)}$  in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop “ $V_F$ ” and hence increase the reverse conduction loss.

### Blocking Voltage

The blocking voltage rating,  $BV_{DS}$ , is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30% higher than the rated  $BV_{DS}$ . As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and doesn't change with negative gate voltage. A transient drain-to-source voltage of 750V for 1  $\mu$ s is acceptable.

### Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the GS66516T device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

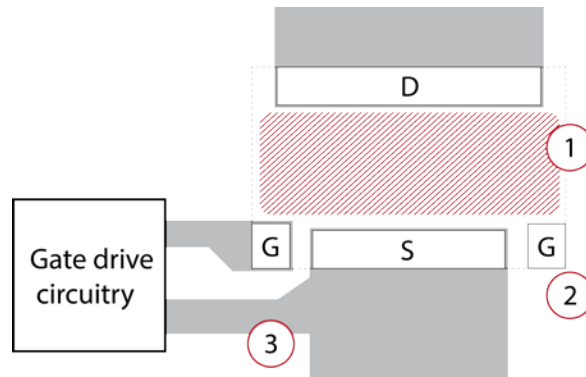
- Preheat/Soak: 60-120 seconds.  $T_{min} = 150$  °C,  $T_{max} = 200$  °C.
- Reflow: Ramp up rate 3°C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using “Non-Clean” soldering paste and operating at high temperatures may cause a reactivation of the “Non-Clean” flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the “Non-Clean” paste residues.

Avoid placing printed circuit board traces with high differential voltage to the source or drain directly underneath the top-cooled GS66516T package on the PCB to avoid potential electro-migration and solder mask isolation issues during high temperature or/and voltage operation.

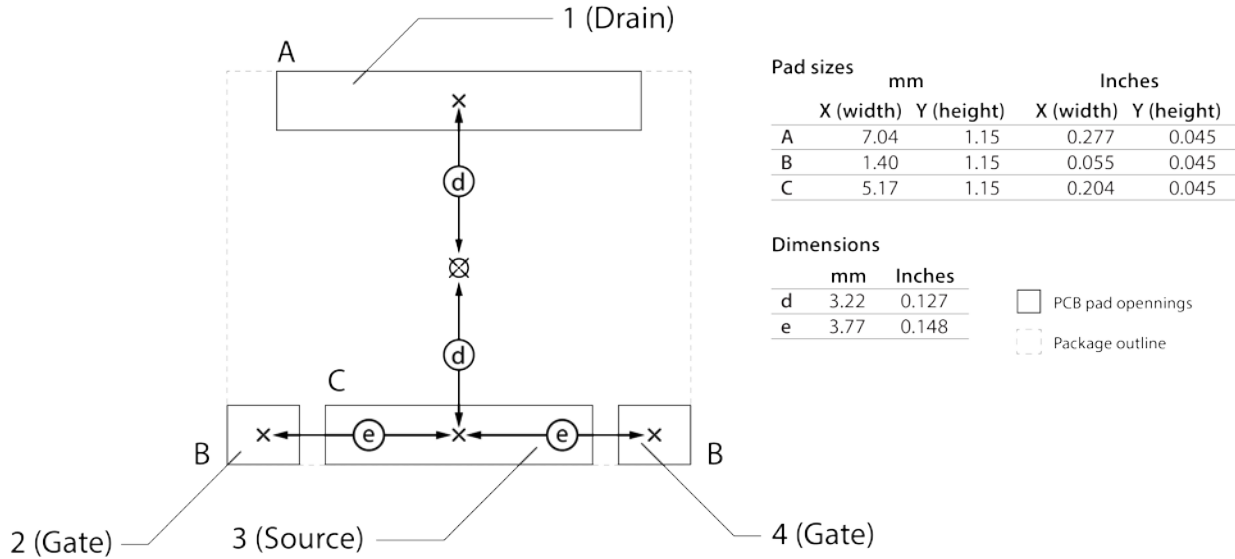
### Routing Guidelines

To avoid common pitfalls in routing the top-side cooled package, the following layout recommendations are highlighted. Additional detail is provided in Application Note GN001 at [www.gansystems.com](http://www.gansystems.com).

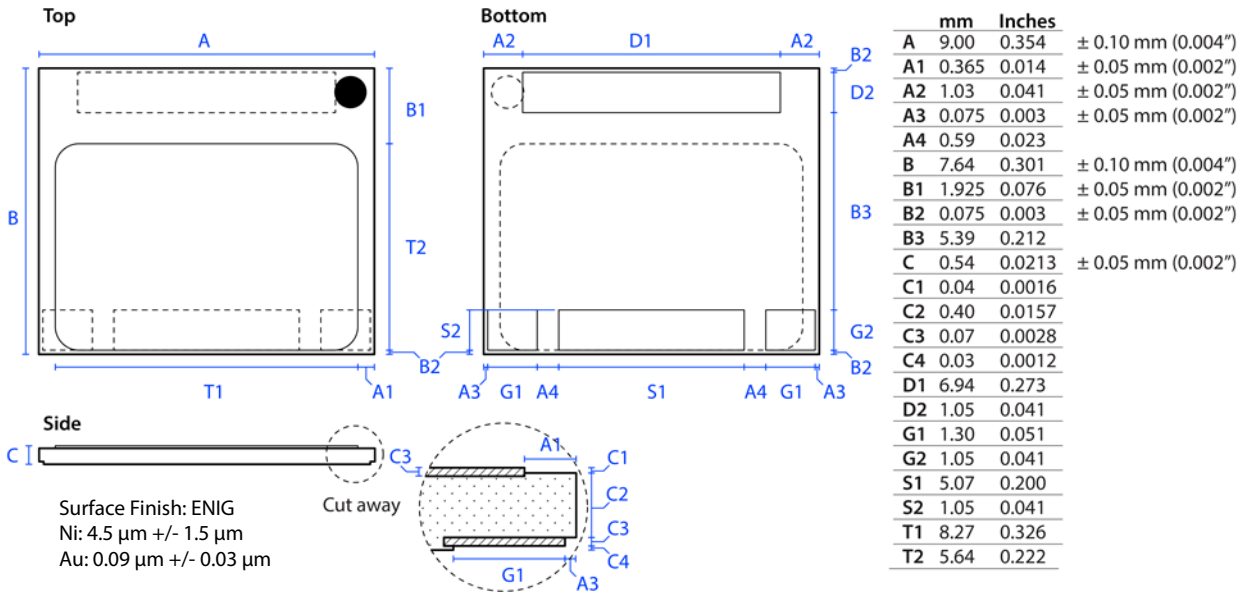


- ① Keep out area: Avoid placing traces or vias on the top layer of the PCB, directly underneath the GS66516T package. This is to prevent potential electro-migration and solder mask isolation issues during high temperature or/and voltage operation.
- ② Symmetrical dual gates are provided for flexible layout and easy paralleling. Either gate drive can be used. If the second gate is not used, it should be left floating.
- ③ A separate Source Sense pin is not provided on our top-side products because of the ultra-low inductance of our GaNPX® packaging. The Source Sense pin functionality can be implemented simply by routing a Kelvin connection at the side of the Source pad. This can be done at either side of the source pad for layout optimization.

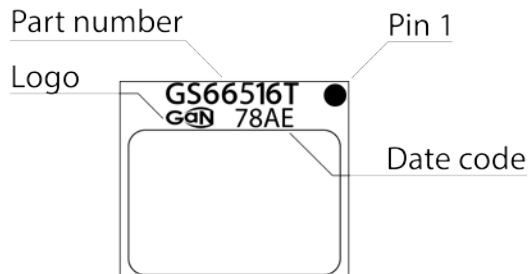
**Recommended Minimum Footprint for Printed Circuit Board**



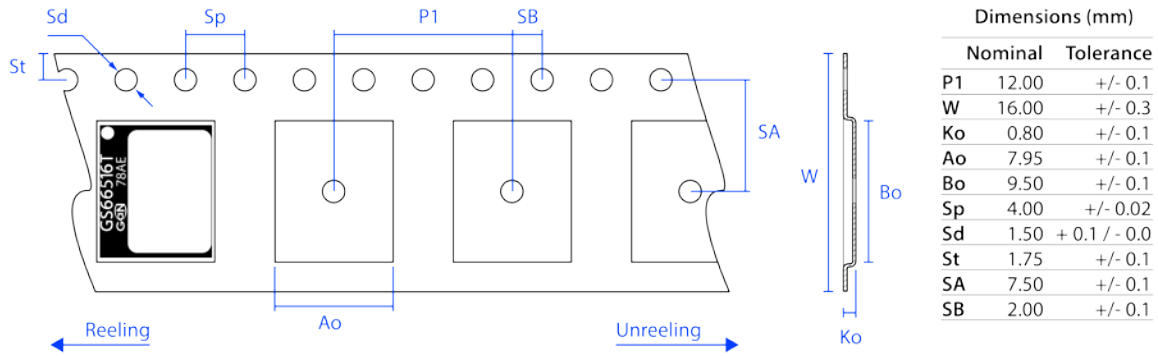
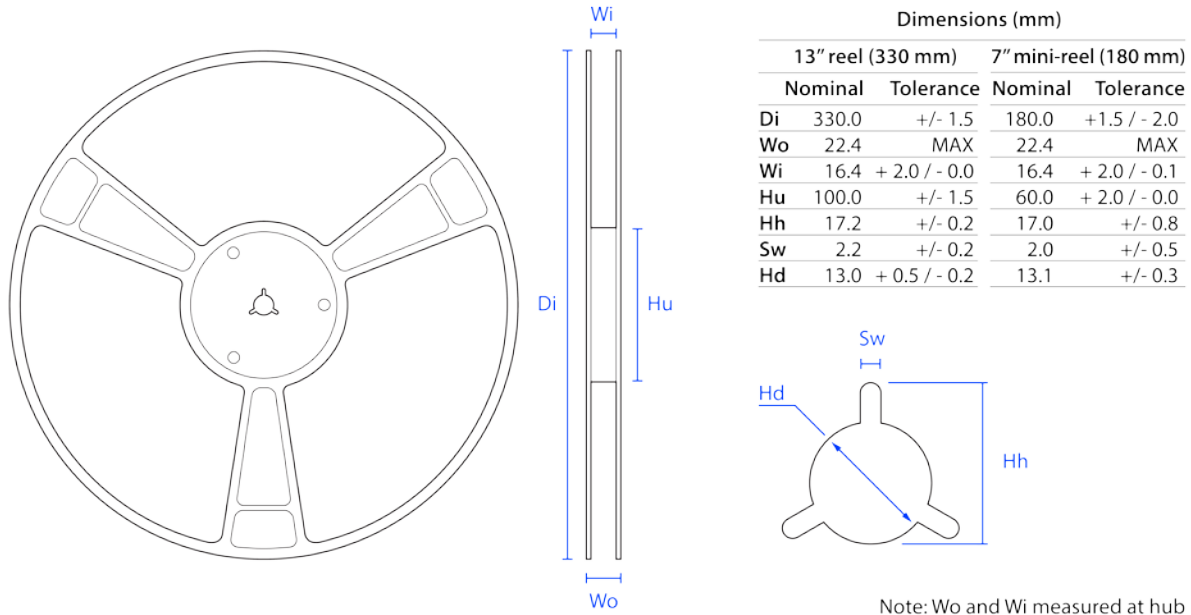
## Package Dimensions



## GaN<sup>PX</sup> Part Marking

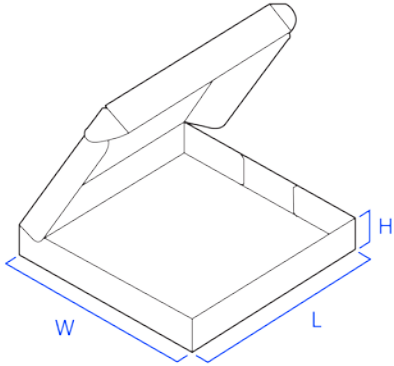


### GS660516T GaNPX® Tape and Reel Information





## Tape and Reel Box Dimensions



Outside dimensions (mm)		
	7" mini-reel	13" tape-reel
<b>W</b>	197	342
<b>L</b>	204	355
<b>H</b>	32	53

[www.gansystems.com](http://www.gansystems.com)

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