Thermal and Electrical Performance of CMOS Driver Compatible GaN Power Transistors

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Abstract
This paper describes the thermal and electrical characteristics of GaN on SiC power transistors that have been designed to be mounted directly upon a CMOS driver integrated circuit. In order to maximize the customer value proposition and minimize the cost implications of using a high capability GaN on SiC die, the hybrid device has to exhibit substantial performance and convenience advantages over a simple cascode structure based upon discrete transistors. The design was also directly influenced by the very complex and costly discrete component PCB based driver designs needed by SiC and IGBT power devices. The size, cost and inconvenience of these driver designs arises from the very high discrete component count, which may reach triple digits for the half bridge configuration. This paper describes the design of the GaN transistor and a compatible CMOS driver. This new self powered integrated structure reduces the external component count to single digit totals. In this paper, methods are discussed for modeling and validating each step of the product development.

INTRODUCTION

GaN-based power transistors are attractive power switching devices [1]. The conventional AlGaN/GaN HEMT structure is a well proven construct, but the resulting device is normally-on and this is inconvenient for switching applications. The usual solution is to employ a discrete MOSFET to provide a switch in series with the GaN transistor. This cascode arrangement enables normally-off operation. Performance improvements and additional features can be incorporated if the required normally-off MOSFET is made part of a CMOS integrated driver. To allow for this possibility, the on-resistance of the integrated MOSFET needs to be comparable with the discrete alternatives. Using a low cost 1 micron CMOS process it was determined that a 8-18 mOhm MOSFET could be achieved in an area of less than 4x4 mm². Given that GaN devices operating at 650/900/1200V to provide for example an 80 to 180 mOhm on-resistance the MOSFET will therefore add minimal additional on-resistance.

The proprietary GaN transistor array developed uses solder tipped copper posts which are plated upon 12 islands that connect to each of the GaN transistor’s separate source electrodes. A post is also provided for the gate electrode. The drain electrodes are connected to the back of the die with 12 through-wafer vias. The devices were designed for 650, 900 and 1200V system use; they are 2x2mm² and capable of 40/30/20A operation (Figure 1).

Figure 1. GaN transistor with solder tipped copper posts.

Although the GaN die is thinned to 100 microns, thermal resistance remains a concern. Heat removal from the GaN die is achieved separately from the heat that is generated by the MOSFET. This approach is needed to allow the MOSFET to remain within its temperature range. Therefore packaging issues were a prime concern during the design process (Figure 2).

Figure 2. The PQFN package provides the two separate heat spreading thermal electrodes that are needed for thermal integrity.
THERMAL RESISTANCE

Because the GaN transistor has ten times the on-resistance of the MOSFET it is vital to achieve effective heat removal from the surface of the GaN device. Although there are 12 plus 1 copper posts mounted on the surface of the GaN transistor, more than 90% of the heat is actually dissipated via the substructure of the GaN transistor. Currently most GaN transistors produced are built on SiC or Si substrates. Devices produced using thick Si substrates are less prone to warp issues but the thermal resistance is problematic. However, if Si substrates can be thinned to 0.1mm, the thermal resistance of the SiC and the Si substrates are similar, as shown. The graphs shown were drawn for the example where the GaN device dissipates 40W and CMOS device dissipates 4 Watts. The upper and lower heat spreaders are held at 50°C. The combined devices 2x2mm GaN and 4x4mm CMOS are mounted in an equivalent PQFN structure outlined in the thermal cross section (Figure 3).

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CMOS / GaN DRIVER SUB-SYSTEM

The CMOS driver design follows the basic structure of differential CMOS line receivers. The differential inputs have associated Schmitt triggers circuits and a lockout latch ensures that the circuit can discriminate against non-differential inputs. The combination allows the driver to provide a clean drive signal to the pre-driver even when the circuit is used in a high noise environment. The input circuits therefore provide the truth table function shown; the resulting signal is used to enable the output of the cascade of inverters. The final inverter is sufficiently sized to drive the large MOSFET structure connected in series with the GaN transistor (Figure 4).

Figure 4. Self Powered Driver with lock-out latch function.

While the overall functionality follows that of conventional differential line receivers, additional and critically significant circuitry is needed to ensure convenient and safe operation. The complete circuit function has to incorporate a self-power capability and a safety lockout circuit. The design gathers power from the bespoke GaN power device and also the input power that can be further harvested from the pulse transformer. The transient nature of these power sources raises serious issues that dictate the need for a safety lockout circuit with triple redundancy. The power switch must remain off during the control power-up and power-down events. Safe and convenient operation is achieved by this unique and proprietary circuit. This is the key advantage of this design concept. It is important to compare the simplicity of this design with the complexity of PCB discrete component driver designs used by SiC and IGBT power switch devices. The exceptionally high mutual conductance of normally-on GaN devices is the vital enabling factor. Previously the normally-on nature of the GaN transistor, and its negative threshold voltage, was regarded as a disadvantage; here it is an advantage because it allows for low voltage CMOS cascode drive and control. Advanced functionality and protection circuits can be further added to the CMOS control chip.
THE COMBINED SYSTEM

The CMOS circuit was designed to conform to the design rules of a conventional 1 micron CMOS fabrication foundry. SPICE models were supplied by the CMOS foundry and a SPICE model was developed for the GaN transistor. Particular care was taken to include within the GaN model a thermal network that includes several elements that enable the on-resistance and saturation current to dynamically track active area temperature. The model includes the thermal resistance of the GaN transistor and it also allows the user to include the package thermal resistance (Figure 5).

![Block diagram illustrating the elements used in the electro-thermal non-linear model developed for the GaN HEMT.](image)

Keeping the model compact, and restricting it to a small number of nodes, allows for quick convergence in highly non-linear simulations such as power switching transients. In order to populate the model parameters with appropriate values, the GaN device has been characterized using pulsed IV and CV measurements over bias and temperature. Consideration was given to process corners and statistical variations. Systematic verification of the device behavior under various modes of operation, including power switching load lines, completes the modeling process. Co-simulating the transient response of the GaN transistor with the CMOS driver and the package parasitics provides a realistic prediction of the electrical and thermal performance of the device in a power switching application. The CMOS / GaN hybrid was designed to be capable of being driven by an isolating pulse transformer. Galvanic isolation allows for the device to be used in the upper section of a half bridge. This isolation, if achieved at low cost can also be used to alleviate ground loop problems that may occur when driving the lower section. The simulated results include the pulse transformer SPICE model. The delay from the rise of the input to the Schmitt circuit to the MOSFET turning-on is less than 5nS. The GaN transistor is fully on within 40nS of the input signal to the Schmitt trigger reaching 3 volts. The input capacitance of the Schmitt circuits is less than 1pF (Figure 6).

![Simulated device results including pulse transformer, CMOS circuit and GaN transistor.](image)

MEASURED RESULTS

![The screen shot shows the output transitions.](image)

The GaN transistor and CMOS circuit were assembled in a prototype PQFN package. Given a resistive load of 60 Ohms the 1200V GaN transistor cascoded with the CMOS / MOSFET is able to achieve a 350V transition within 10nS. The delay from the predriver transition to the completed output swing is less than 15nS. The overall delay time from the output of the isolating pulse transformer is approximately 20nS – the CMOS circuit having added 5nS (Figure 7).
CONCLUSIONS

In this paper, Hybrid CMOS/GaN 650/900/1200 Volt power switching devices have been described. The CMOS IC and the GaN transistors use conventional 1 micron foundry technology. The unique island layout scheme allows the lateral GaN transistor, currently built using a SiC substrate, to be conveniently transferred to GaN on Si foundry facilities as they become available. This will provide substantial cost savings initially for the 650V GaN transistor and later for the 900 / 1200V GaN transistors.

The CMOS driver evolution is centered upon achieving isolated drive and self-power capability in the near term and later, short circuit protection with monitoring capability for temperature, over voltage and over current. These improvements provide for enhanced customer value.

In addition, the concept of providing a proven closed system that shields the user from the safety issues is especially attractive.

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REFERENCES


